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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,481	02/20/2004	Tae-joong Song	5649-1235	1306

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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,481	SONG, TAE-JOONG	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *13-21 and 26-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8-11,22,23 and 25* is/are rejected.

7)☒ Claim(s) *4,7,12 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Response filed March 17, 2006 has been entered.

Drawings

2. The replacement drawings, figs. 2 and 5 (Ex. D) were received on March 17, 2006. However, these drawings are not acceptable for being non-compliant.

The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

3. In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations indicating the changes made to the previous version. The marked-up copy must be clearly labeled as "Annotated Sheets" and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37 CFR 1.121(d)(1). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

Response to Arguments

4. Applicant's arguments with respect to claims 1 – 3, 5, 6, 8, 9, 11, 22, 23, and 25 have been considered but are moot in view of the new ground(s) of rejection that follow.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 3, 5, 6, 8, 9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Jung, Y H (KR 2002054857 A).

Regarding **claims 1 – 3, 5, 6, and 9,** AAPA discloses a semiconductor memory device, comprising:

a memory cell array having a plurality of memory cells, a plurality of word lines, and first and second bit lines (fig. 1, paragraph 0004);

an address decoder which decodes a received address signal, wherein the address decoder is coupled to the plurality of word lines (fig. 2, 210); and

a precharge unit that precharges the first and second bit lines in response to the precharge signal (fig. 2, unit 230), wherein the precharge unit comprises:

first and second transistors which in response to the precharge signal precharge the first and second bit lines, respectively, to a power supply voltage level (fig. 2, PMOS transistors 232 and 234, see also paragraph 0029); and

a third transistor which in response to the precharge signal equalizes the voltage of the first and second bit lines (fig. 2, PMOS transistor 236, paragraph 0029),

wherein the address decoder is a row address decoder and wherein the decoded address signal comprises a row address (paragraph 0008, decoder 210 in fig. 2 is a row decoder. Inherently, address that is decoded from the row decoder is a row address).

Although AAPA did not clearly show the semiconductor memory device further comprising a precharge control circuit that generates a precharge signal in response to a precharge enable signal and a precharge delay signal that is generated by a delay circuit for a predetermined delay time, wherein the address decoder is a row address decoder and the decoded address signal comprises a row address (as additionally entailed in claims 1 – 3 and 9), the features are however shown by Yung, Y H, as can be seen according to the figure drawing.

Precharge control signal generator circuit (figure) generates precharge signal MAPCih (output of inverter 55) in response to a *precharge enable signal* (YIOR) and a *precharge delay signal* (any signals from one of delay circuits 41, 44, 47, or 52). The semiconductor device further comprises a *delay circuit* (47) for generating the precharge delay signal by delaying the precharge enable signal YIOR for a predetermined delay time (propagation delay through the first delay portion delay circuit 41). The precharge control circuit comprises a *NAND gate* (top NAND gate of latch portion 54), which receives the precharge enable signal (propagated signal YIOR through NAND gate 45) and the precharge delay signal (propagated delay signal from

delay circuit 47 through the bottom NAND gate of the latch portion 54), which is responsive to the delay circuit 47. The precharge control circuit also comprises *an inverter* 55, which inverts the output of the NAND gate (the top NAND gate of latch 54).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the features taught by Yung to the AAPA to provide a controlled precharge signal to prevent a malfunction of a main amplifier (see novelty).

Regarding **claim 8**, Yung also shows the semiconductor of claim 2, wherein the precharge control circuit (figure) generates the precharge signal (output from inverter 55) by performing a logical AND operation (output signal from inverter 50, which inverts the output signal from NANd gate 49, which constitutes a logical AND operation—similar to that of fig. 4 of the instant application) on the precharge enable signal (YIOR) and the precharge delay signal (output from delay portion 47).

Regarding **claim 11**, it is considered inherent given the precharge circuit of the figure drawing by Yung, that the signal output MAPCih at the output of inverter 55 is disabled **a predetermined time after the precharge enable signal is disabled** due to inherent propagation delay of signals YIOR through circuits the entire circuit.

8. Claims 10, 22, 23, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) and Jung, Y H, and further in view of Houston (US Pat Pub 2001/0052624 A1).

Regarding **claims 10, 22, 23, and 25**, AAPA and Yung disclose a method (as inherent) for pre-charging the first and second bit lines of a memory cell array as shown

above (see grounds for the rejection of claims 1, 2, and 11 in paragraph 6 above), except wherein the precharge signal is disabled **after** the word line is enabled. However, this feature has been taught by Houston (paragraph 0057 discloses the step of turning off the bit line precharge after the step of enablement of the word line).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature shown by Houston to the teachings of AAPA and Yung, for which a write back is implemented in the read cycle to prevent susceptibility of memory cell to upset on read (paragraph 0056).

Allowable Subject Matter

9. **Claims 4, 7, 12, 24** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is an examiner's statement of reasons for allowance:

The prior arts of record fail to teach or reasonably suggest the semiconductor memory device, such as disclosed above, wherein the predetermined delay time comprises the time it takes the word line to become enabled in response to a transition of the decoded address signal. In other words, the precharge signal is disabled the predetermined delay time after the word line is enabled (as disclosed in claims 4, 12, and 24, illustrated by fig. 5).

The prior arts of record also fail to teach the delay circuit comprising a NOR gate which receives the precharge enable signal, and an inverter which inverts the output of the NOR gate (as claimed in claim 7 and fig. 5).

11. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D Pham
April 14, 2006

AMIR ZARABIAN
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